WHAT IS CLAIMED IS:

1. A method of measuring phase margin of a delay-locked loop (DLL) having a reference input, the method comprising:

(a) applying a reference clock to the reference input;

(b) providing an auxiliary variable delay within the DLL;

(c) varying the auxiliary variable delay until the DLL becomes unstable; and

(d) generating a phase margin output related to the phase margin as a function of a value of the auxiliary variable delay at which the DLL becomes unstable.

2. The method of claim 1 wherein:

step (b) comprises providing an auxiliary delay line within a delay loop in the DLL, wherein the auxiliary delay line comprises a delay input, a delay output and a plurality of delay cells which are coupled together in series with the delay input; and

step (c) comprises multiplexing outputs of respective ones of the delay cells to the delay output.

3. The method of claim 2 wherein step (c) further comprises:

(c)(1) providing a counter having a count output;

(c)(2) multiplexing the outputs of respective ones of the delay cells to the delay output based on the count output; and

(c)(3) repetitively incrementing and decrementing the count output.

4. The method of claim 3 wherein step (d) comprises:

(d)(1) generating a phase margin output related to the phase margin as a function of the count output at which the DLL switches between a phase-locked state and a phase-unlocked state.

5. The method of claim 4 wherein step (d) further comprises:

(d)(2) generating a lock detect signal having a first logic state when the DLL is in the phase-locked state and a second, different logic state when DLL is in the phase-unlocked state; and

(d)(3) latching the count output when the lock detect signal switches between the first and second logic states.

6. The method of claim 1 wherein:

step (b) comprises providing an analog voltage-controlled delay element within the DLL, which has a control voltage input; and

step (c) comprises applying a control voltage to the control voltage input and varying the control voltage.

7. The method of claim 6 wherein varying the control voltage comprises varying the control voltage such that the control voltage forms a triangular waveform over time.

8. The method of claim 7 wherein the generating step (d) comprises:

(d)(1) generating a lock detect signal having a first logic state when the DLL is in a phase-locked state and a second, different logic state when DLL is in a phase-unlocked state; and

(d)(2) generating the phase margin output as a function of a duty cycle of the lock detect signal as the control voltage is varied over time.

9. The method of claim 8 wherein step (d)(2) comprises:

(d)(2)(i) low-pass filtering the lock detect signal to produce a filtered lock detect signal having a DC voltage;

(d)(2)(ii) comparing the DC voltage with a reference voltage level to produce a comparison output; and

(d)(2)(iii) generating the phase margin output as a function of the comparison output.

10. The method of claim 1 wherein the DLL is embedded within an integrated circuit and wherein the method further comprises:

(e) activating a built-in self-test state machine which is embedded within the integrated circuit and adapted to perform step (c); and

(f) reading the phase margin output with the built-in self-test state machine and generating a self-test output from the state machine that represents functionality of the DLL based on the phase margin output.

11. A delay-locked loop (DLL) comprising:

a reference input;

a feedback input;

a DLL output which is coupled to the feedback input;

a phase detector coupled to the reference input and the feedback input and having a phase control output;

a charge pump coupled to the phase control output;

a loop filter coupled to an output of the charge pump;

a main variable delay element coupled between the reference input and the DLL output and

having a first control input coupled to the loop filter;

an auxiliary variable delay element coupled in series with the main variable delay element, between the reference input and the feedback input, and having a second control input and an auxiliary delay that is variable to a critical delay at which the DLL becomes unstable; and

a phase margin measurement circuit which generates a phase margin output based on the critical delay at which the DLL becomes unstable.

12. The DLL of claim 11 wherein the auxiliary variable delay element comprises:

an auxiliary delay input;

an auxiliary delay output;

a plurality of delay cells coupled together in series with the auxiliary delay input; and

a multiplexer comprising a plurality of multiplexer data inputs coupled to respective outputs of the plurality of delay cells, a multiplexer data output coupled to the auxiliary delay output and a select control input.

13. The DLL of claim 12 wherein the phase margin measurement circuit comprises:

a counter having a count output coupled to the select control input; and

an output latch having a latch input coupled to the count output, a latch output, and a latch control input.

14. The DLL of claim 13 wherein the phase margin measurement circuit further comprises:

a lock detect circuit having clock inputs, which are coupled to respective ones of the reference input and the feedback input, and a lock output coupled to the latch control input, wherein the lock output has a first logic state when the DLL is in a phase-locked state and a second, different logic state when DLL is in a phase-unlocked state.

15. The DLL of claim 11 wherein the auxiliary variable delay element comprises:

an analog voltage-controlled delay element having a control voltage input; and

a control voltage generator having a control voltage output coupled to the control voltage input.

16. The DLL of claim 15 wherein the control voltage generator generates a control voltage on the control voltage output that has a triangular waveform over time.

17. The DLL of claim 16 wherein the phase margin measurement circuit comprises comprises:

a lock detect circuit having clock inputs which are coupled to respective ones of the reference input and the feedback input and a lock output which has a first logic state when the DLL is in a phase-locked state and a second, different logic state when DLL is in a phase-unlocked state;

a low-pass filter having a filter input coupled to the lock output and having a filter output; and

a comparator having a first comparator input coupled to the filter output, a second comparator input coupled to the a reference voltage and a comparator output, which is indicative of the phase margin.

18. A delay-locked loop (DLL) comprising:

a reference input for receiving a reference signal;

a feedback input for receiving a feedback signal;

a DLL output coupled to the feedback input;

first variable delay means coupled between the reference input and the DLL output for providing a first variable delay;

phase control means for detecting a phase difference between the reference signal and

the feedback signal and for varying the first variable delay as a function of the phase difference; and

phase margin measurement means for adding further delay in series with the first variable delay means, between the reference input and the feedback input, and for generating a phase margin output as a function of an amount of the further delay that is required for the DLL to become unstable.